| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 76 | "714"/$.ccls. and (DMA (direct adj memory adj access)) with test$5 near4 (memory ram rom storage cache) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 16:04 |
| S1 | 6 | "5423029" and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and DMA and (ram rom memory storage) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/05 14:28 |
| S2 | 1 | "5423029" and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and DMA and (ram rom memory storage) and test and module | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/05 14:30 |
| S4 | 5160 | (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:30 |
| S5 | 344 | direct adj2 tv | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:31 |
| S6 | 195 | (direct adj2 tv) and satellite | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:32 |
| S7 | 30 | (direct adj2 tv) and satellite and internet and account and record | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:43 |
| S8 | 3 | (direct adj2 tv) and satellite and internet and account and record and telemetry | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:33 |
| S9 | 1850101 | (direct adj2 tv) and satellite and internet and account and record and malfunction near$4 (satellite spacecraft) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:48 |

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| S10 | 11 | "5940739" | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:51 |
| S11 | 9211547 | "10"/ "023892" | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:51 |
| S12 | 4 | "10023892" | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:52 |
| S13 | 2 | "20020095270" | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 09:52 |
| S14 | 1 | "5423029" and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/09 16:13 |
| S15 | 4 | ("5423029" "5446741" "6480982" "5668815") and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 16:28 |
| S16 | 1 | ("5423029" "5446741" "6480982" "5668815") and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 14:38 |

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| S17 | 2322 | (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 14:38 |
| S18 | 7 | "324"/$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 14:42 |
| S19 | 44 | "702"/$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 15:10 |
| S20 | 8 | "73"/$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 14:42 |
| S21 | 37 | "702"/$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) near4 (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module and slot | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 15:13 |
| S22 | 27 | "702"/$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (I/O or (input near2 output)) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and (test near3 (module slot card)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 15:15 |

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| S23 | 52 | 714/9,42,702,718.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 16:28 |
| S24 | 12 | 714/9.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and input and output and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test and module | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 16:32 |
| S25 | 2 | 714/9.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test near2 (card module) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/23 18:09 |
| S26 | 120 | "714"/$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test near2 (card module) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 16:41 |
| S27 | 91 | "714"/$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test adj2 (card module) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/10 17:16 |
| S28 | 8 | "714"/$.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test adj2 (card module) and expansion near2 slot | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/11 17:01 |

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| S29 | 26 | (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test adj2 (card module) and expansion near2 slot and (operating adj2 system) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/11 17:06 |
| S30 | 0 | (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test adj2 (card module) and expansion near2 slot and (operating adj2 system) and (bus adj2 bridge) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/11 17:07 |
| S31 | 8 | 714/9,25.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test near2 (card module) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/25 14:38 |
| S32 | 1 | 717/105.ccls. and (microprocessor processor controller microcontroller CPU computer microcomputer) and (input near2 output) and (DMA (direct near4 memory near4 access) (bus near4 master near4 transfer)) and (ram rom memory storage) and test near2 (card module) and bus and system and error and slot$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/08/09 13:33 |
| S39 | 74 | "5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373" | USPAT | OR | OFF | 2005/08/09 14:14 |
| S40 | 5 | ("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O same controller same dma | USPAT | OR | OFF | 2005/08/09 14:16 |
| S41 | 6 | ("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O and controller and dma | USPAT | OR | OFF | 2005/08/09 14:16 |
| S42 | 3 | ("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O and controller and dma and test | USPAT | OR | OFF | 2005/08/09 14:16 |

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| S43 | 2 | ("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O and controller and dma and test same (module card device) | USPAT | OR | OFF | 2005/08/09 14:17 |
| S44 | 3 | ("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373") and I/O and controller and dma and test same (module card device) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 10:34 |
| S45 | 3 | ("5396619" "2003065470" "5621886" "5446741" "5619513" "5668815" "20030005373" "5621883" "2214671" "2268295" 98/07163) and I/O and controller and dma and test same (module card device) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 10:40 |
| S46 | 2 | "20030005373".pn. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 10:40 |
| S47 | 4 | "20030005373".pn. "56199513".pn. "5668815".pn. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 10:50 |
| S48 | 0 | (DMA (direct adj memory adj access)) same (exapansion near5 slot) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 10:51 |
| S49 | 108 | (DMA (direct adj memory adj access)) same (expansion near5 slot) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 10:52 |
| S50 | 3 | (DMA (direct adj memory adj access)) same (expansion near5 slot) with test | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 10:54 |

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| S51 | 5 | (DMA (direct adj memory adj access)) same (expansion same slot) with test | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 11:01 |
| S52 | 7 | (DMA (direct adj memory adj access)) same (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test$4 near4 card$2 and test$5 near6 (memory ram rom storage) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 11:06 |
| S53 | 7 | (DMA (direct adj memory adj access)) same (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test$4 near4 card$2 and test$5 near6 (memory ram rom storage cache) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 12:38 |
| S54 | 39 | (DMA (direct adj memory adj access)) and (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test$4 near4 card$2 and test$5 near6 (memory ram rom storage cache) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 12:38 |
| S55 | 35 | (DMA (direct adj memory adj access)) and (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test$4 near4 card$2 and test$5 near4 (memory ram rom storage cache) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 14:09 |
| S56 | 9 | "714"/$.ccls. and (DMA (direct adj memory adj access)) and (ISA, EISA, VESA, PCI, AGP, AMR,CNR slot) same test$4 near4 card$2 and test$5 near4 (memory ram rom storage cache) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/08/10 16:04 |